REMARKS IN RESPONSE

Claims 1-6 and 8-19 are pending in the application.

Claims 2, 12 and 15 have been deleted.

Claims 1, 3, 5, 8, 11, 13, 14, 16, 17 and 19 have been amended, as set forth above.

I. OBJECTIONS TO THE DISCLOSURE AND DRAWINGS

Applicants have amended a section of the Brief Description of Drawings as noted by the Examiner.

Applicant respectfully traverses the Examiner's requirement that the term "delta" should be strictly defined. This term is common in the art, and a person of ordinary skill in the art knows the meaning of the term -- difference.

Applicant respectfully traverses the Examiner's requirement that the reference "TO OTHER CIRCUITRY" in FIGURE 4C requires description in the specification. FIGURE 4C is clear and the "other circuitry" can be any other circuitry, as desired by those practicing the invention.

With respect to the objection to the drawings, Applicant will correct these deficiencies upon a notice of allowance and shall submit new formal drawings in response thereto with the corrections.

II. REJECTION UNDER 35 U.S.C. § 112

Claims 1-6, 8-10 and 19 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The Examiner's rejection is respectfully traversed.

Applicant has amended Claim 1, line 5 by replacing "a" with "the" prior the second instance of "source". In Claim 19, "respective" has been added to precede "length", as requested by the Examiner.

Accordingly, the Applicant respectfully requests withdrawal of the Examiner's rejection of Claims 1-6 and 8-10.

III. REJECTION UNDER 35 U.S.C. § 102

Claims 1, 8, 9, 11, and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,043, 792 to Adachi. The Examiner's rejection is respectfully traversed. Claim 15 has been canceled.

Independent Claims 1 (and dependent Claims 8 and 9) and 11 have been amended to include a third conductor (as amended). Adachi does not disclose a third conductor as recited in Applicant's Claims 1 and 11.

Accordingly, the Applicant respectfully requests the Examiner withdraw the Section 102(b) rejection of Claims 1, 8, 9, 11 and 15.

IV. REJECTION UNDER 35 U.S.C. § 102

Claims 1-4, 8, 9, 11-15, 17 and 18 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,027,088 to Shimizu, et al. The Examiner's rejection is respectfully traversed. Claims 2, 12, and 15 have been canceled.

Independent Claims 1 (and dependent Claims 2, 4, 8 and 9), 11 (and dependent Claims 12-14) and 17 (and dependent Claim 18) have been amended to recite that the first ends of the three conductors (or conductive portions) are electrically coupled together in the first area of the circuit, but the second ends of the second and third conductors are not coupled in the second area of the circuit. More specifically, amended Claim 1 recites that the second and third conductors each "having a second end unconnected in the second area of the circuit." Amended Claim 11 recites that the invention is structured such that the second ends of the second and third conductors "are not

electrically coupled in the second area of the integrated circuit." Amended Claim 17 recites that the "first ends of the second and third conductive portions are unconnected to the destination." Shimizu, et al. does not disclose Applicants' invention. Shimuzu shows that all ends of the conductors are terminated.

Accordingly, the Applicant respectfully requests the Examiner withdraw the Section 102(b) rejection of Claims 1, 3, 4, 8, 9, 11, 13-14, 17 and 18.

V. REJECTION UNDER 35 U.S.C. § 103

Claims 10 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Adachi and Claims 10 and 16 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over Shimizu, et al. The Examiner's rejection is respectfully traversed.

Applicants have amended independent Claims 1, 11 and 17 to clearly distinguish Applicants' invention over Adachi and Shimizu, et al., and Claims 1, 11 and 17 are believed to be allowable. Therefore, all dependent claims should be allowable as well.

Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection of Claims 10, 16 and 19.

VI. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

1. Page 5, lines 12-20:

FIGURE 3B is a cross-sectional view along line [A-A] 3A-3A of FIGURE 3A;

FIGURES [4A-4C] 4A, 4B, 4C illustrate different configurations or embodiments of the conductor in accordance with the present invention;

FIGURES [5A-5C] 5A, 5B, 5C illustrate cross sectional views of different embodiments of the conductor of the present invention;

FIGURE 6A is a graph illustrating the improvement in rise time (i.e. showing propagation delays) of a signal on a conductor in accordance with the present invention; and

FIGURES [6B-6D] 6B, 6C, 6D illustrate each of the configurations for the signal waveforms shown in FIGURE 6A.

IN THE CLAIMS:

1. (Amended) An apparatus for decreasing the propagation delay time of an electrical signal transmitted from a source along a conductor in a circuit, the apparatus comprising:

a first conductor having a length extending from a first area of the circuit to a second area of the circuit and for carrying an electrical signal, the first conductor having a first end electrically coupled to [a] the source capable of providing the electrical signal and a second end electrically coupled to a destination[; and],

a second conductor having a length extending from the first area of the circuit to the second area of the circuit and located proximate the first conductor and extending substantially parallel and along the first conductor, the second conductor having a first end electrically coupled in the first area of the circuit to the source and having a second end unconnected in the second area of the circuit; and

a third conductor having a length extending from the first area of the circuit to the second area of the circuit and located proximate the first conductor and extending substantially parallel and along the first conductor, the third conductor having a first end electrically coupled in the first area to the source and having a second end unconnected in the second area of the circuit, and wherein the second and third conductors reduce the effective capacitance of the first conductor thereby increasing the speed of the electrical signal when transmitted along the first conductor.

3. (Amended)) The apparatus in accordance with Claim [2] 1 wherein the first conductor, the second conductor and the third conductor are located substantially in a first plane.

5. (Amended) The apparatus in accordance with Claim 3 further comprising [a fourth conductor located proximate the first conductor and extending substantially parallel and along the first conductor, the fourth conductor electrically coupled to the source.] a fourth conductor having a length extending from the first area of the circuit to the second area of the circuit and located proximate the first conductor and extending substantially parallel and along the first conductor, the fourth conductor having a first end electrically coupled in the first area to the source and having a second end unconnected in the second area of the circuit.

8. (Amended) The apparatus in accordance with Claim 1 wherein the first conductor, the second conductor and the third conductor [and the second conductor] each comprise metal.

11. (Amended) An electrical conductor for increasing the speed of an electrical signal transmitted along the conductor in an integrated circuit, the conductor comprising:

a first conductor having a first end in a first area of the integrated circuit and a second end in a second area of the integrated circuit, and having a length extending from the first area to the second area;

a second conductor located proximate the first conductor and having a first end in the first area of the integrated circuit and a second end in a second area of the integrated circuit, and extending substantially parallel and along the first conductor from the first area to the second area[; and],

a third conductor located proximate the first conductor and having a first end in the first area of the integrated circuit and a second end in a second area of the integrated circuit, and extending substantially parallel and along the first conductor from the first area to the second area,

first means for electrically coupling the first end of the first conductor to the first end of the second conductor, and wherein the second end of the first conductor and the second end of the second conductor are not electrically coupled in the second area of the integrated circuit; and

second means for electrically coupling the first end of the first conductor to the first end of the third conductor, and wherein the second end of the first conductor and the second end of the third conductor are not electrically coupled in the second area of the integrated circuit.

13. (Amended) The electrical conductor in accordance with Claim [12] 11 wherein the second conductor and the third conductor are located substantially in a same plane as the first conductor.

14. (Amended) The electrical conductor in accordance with Claim [12] 11 wherein the coupling of the first conductor to the second conductor and to the third conductor decreases the effective capacitance of the first conductor thus decreasing the propagation delay time of an electrical signal when transmitted along the first conductor from the first area to the second area of the integrated circuit.

16. (Amended) The electrical conductor in accordance with Claim [15] 11 wherein the length of the first conductor is greater than about 1000 microns.

17. (Amended) A conductor for transmitting a clocking signal from a first area to a second area of an integrated circuit, the conductor comprising:

a first elongated conductive portion having a first end and a second end extending from the first area to the second area[;],

a second elongated conductive portion having a first end and a second end and located proximate and space apart from the first conductive portion and extending substantially parallel with the first conductive portion from the first area to the second area[;],

a third elongated conductive portion having a first end and a second end and located proximate and space apart from the first conductive portion and extending substantially parallel with the first conductive portion from the first area to the second area[;],

means for electrically connecting the first end of the first conductive portion to the first end of the second conductive portion[;],

means for electrically connecting the first end of the first conductive portion to the first end of the third conductive portion[; and],

a source located within the first area and coupled to the first ends of the first, second and third conductive portions and capable of generating a clocking signal for transmission on the first conductive portion from the first area to the second area; and

wherein the first end of the first conductive portion is connected to a destination in the second area, and the first ends of the second and third conductive portions are unconnected to the destination.

19. (Amended) The conductor in accordance with Claim 18 wherein the respective length of each of the first conductive portion, the second conductive portion, and the third conductive portion is greater than about 1000 microns.

Applicant respectfully requests the Examiner call the undersigned attorney at the below listed number if the Examiner believes it would be helpful in resolving any remaining issues.

The Commissioner is hereby authorized to charge any additional fees connected with this paper or credit any overpayment to Deposit Account No. 19-1353.

Respectfully submitted,

Attorney for Applicants

Date: 03/04/2002

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